

Wall-Temperature Limits for Sn in ARIES-RS/AT and Modeling for NSTX Li Module*

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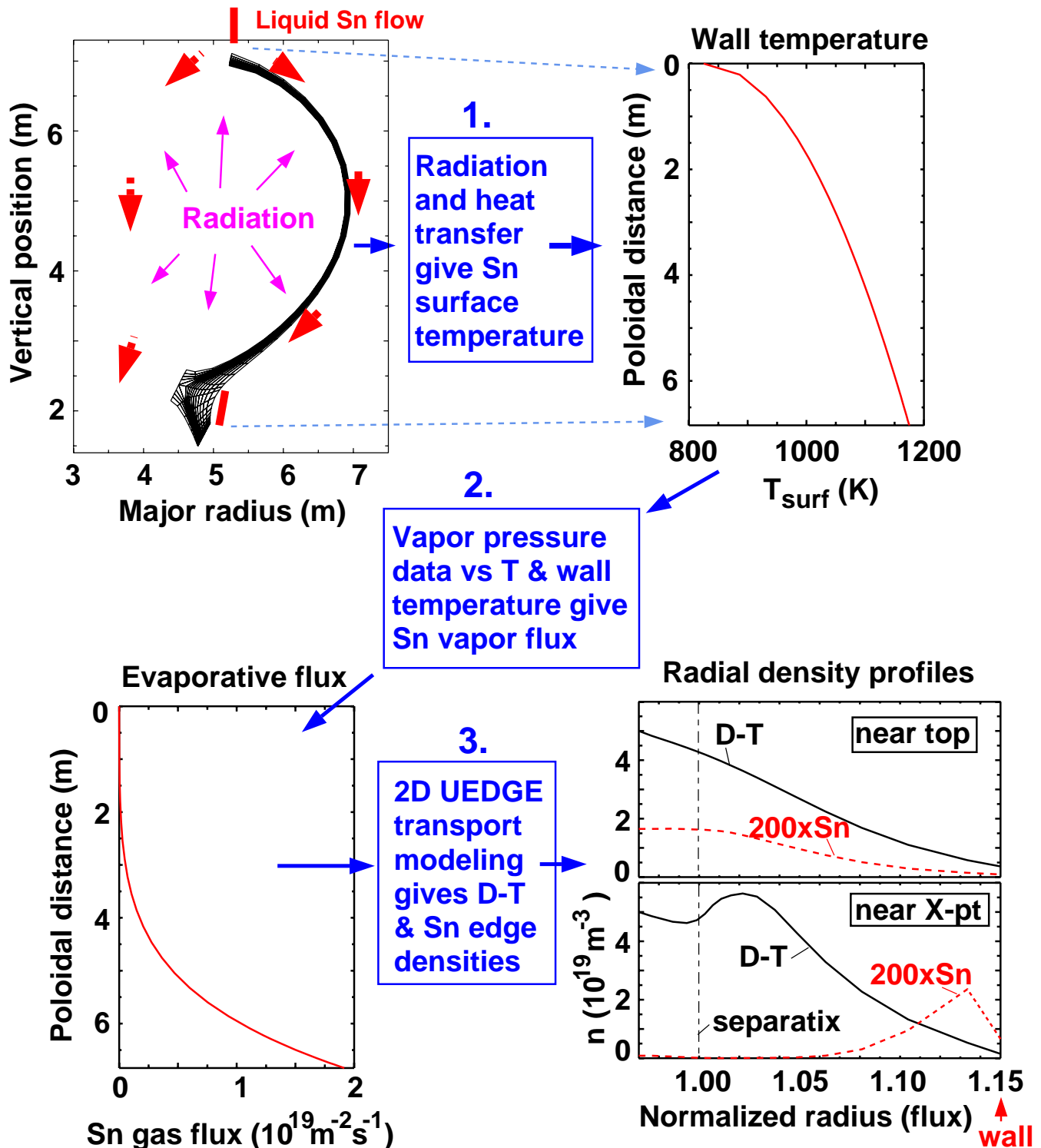
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A systematic set of steps predicts the core impurity level from liquid walls



An acceptable core Sn level is obtained for ARIES case:



Summary of core-impurity-based surface temperature limits for tokamaks

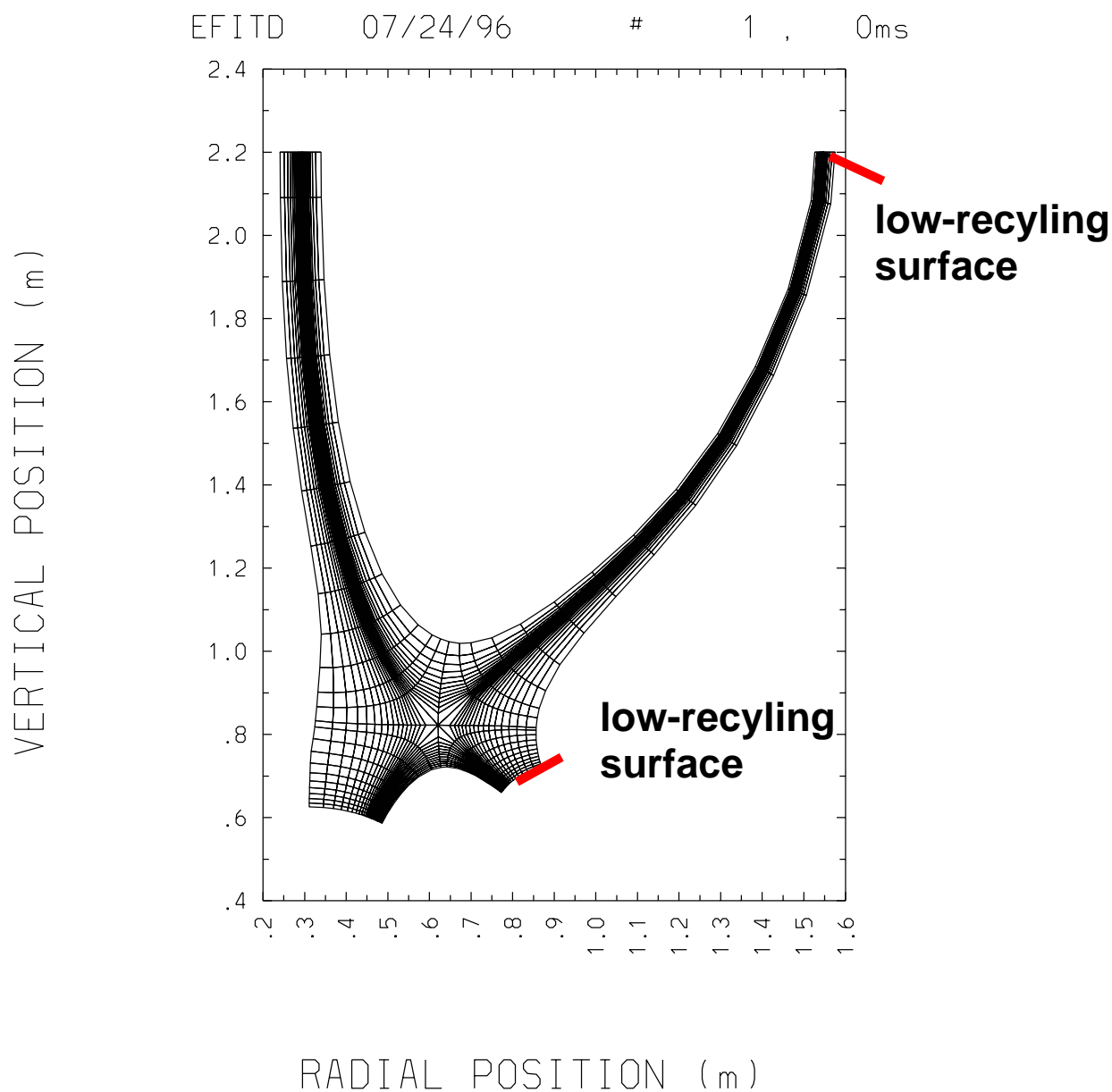
No auxiliary impurity removal scheme used

Red numbers imply same wall/divertor material

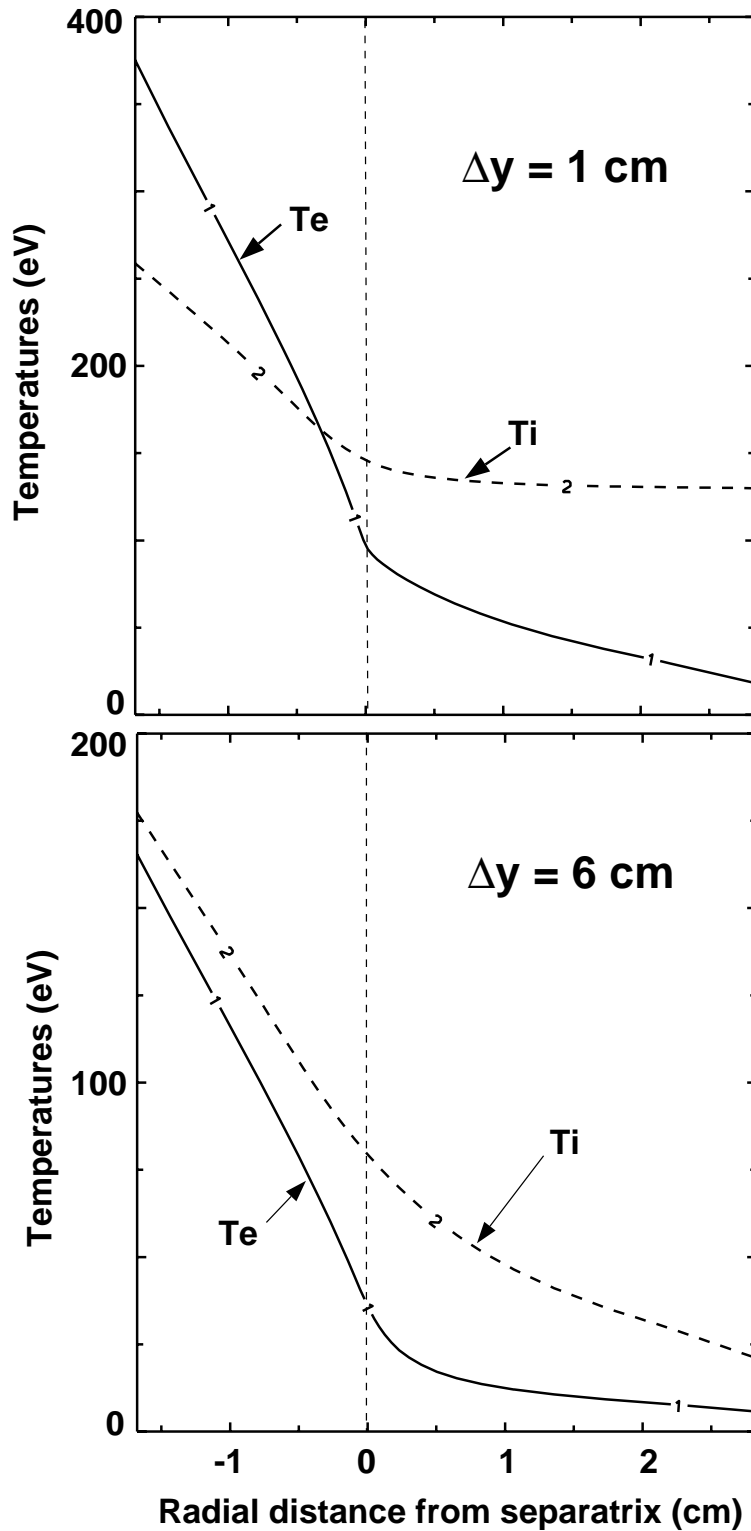
Hydrogen recycling	Lithium °C	Flibe (F) °C	Sn ₈₀ Li ₂₀ °C	Sn °C
$R_h = 0.25$	380	480	590	> 850
$R_h = 0.99$	> 300	400 (solid)	> 500	830

Effective wall temperatures are quoted as determined by the total acceptable impurity flux; e.g., for Sn, the inlet is 550 C and the outlet is 900 C.

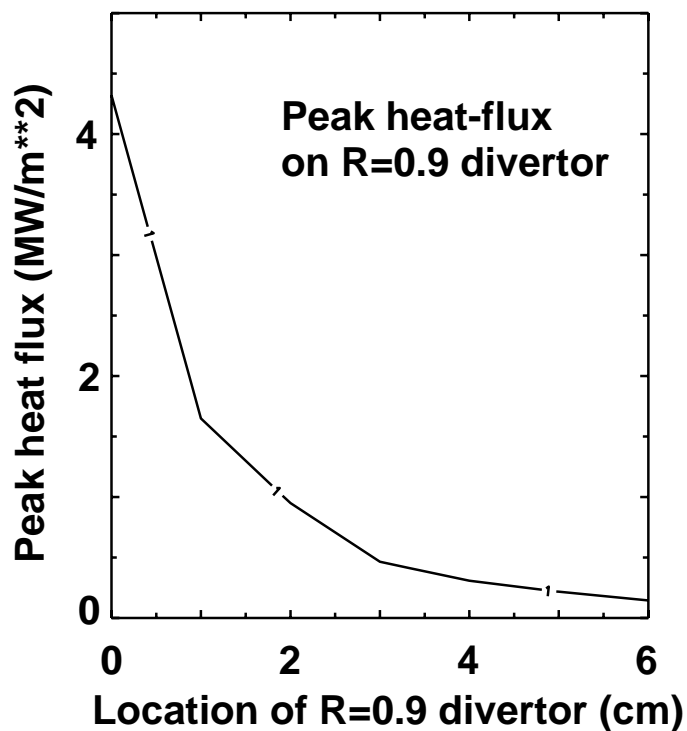
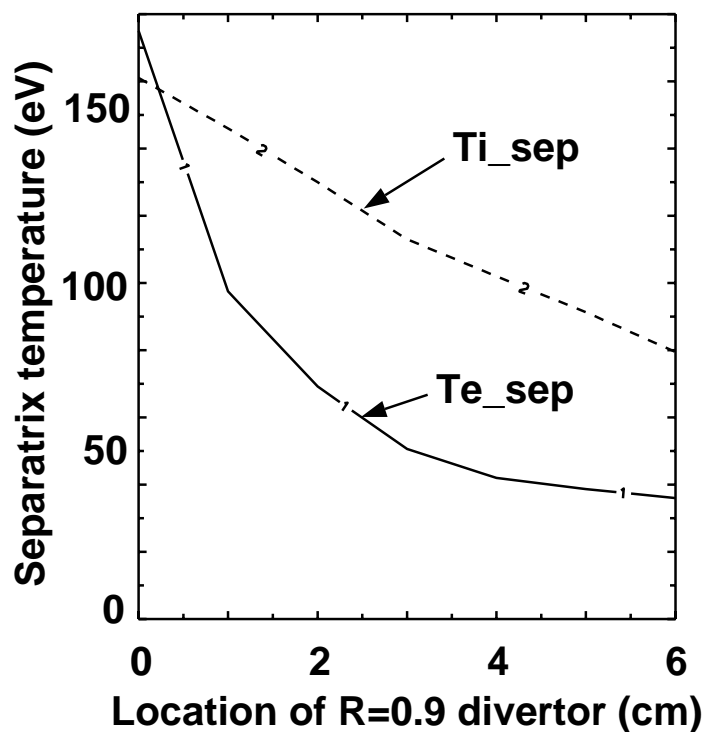
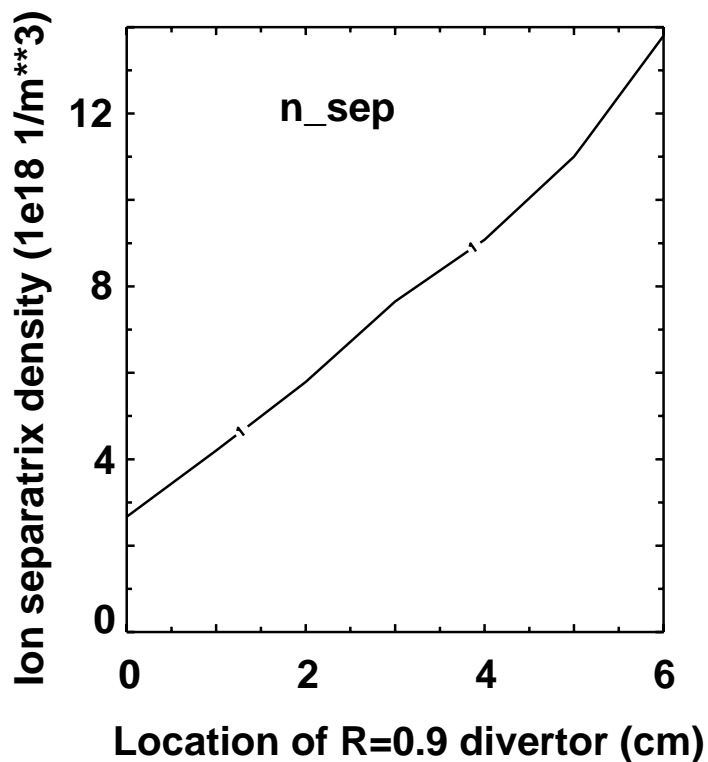
Initial NSTX double-null configuration (EFIT case k22_d035_li055)



Midplane temperatures for two locations of $R=0.9$ low recycling plate; $I_{core}=100$ A



Edge plasma varies with location of R=0.9 divertor



Plans for edge-plasma modeling



- Analyze impact of divertor shape on heat load and helium pumping efficiency
- Evaluate the wall temperature limits for galium
- Continue modeling for NSTX module and possibly other devices
- Assist with CDX-U modeling - bottom limiter